IN THE SPECIFICATION:

Please amend the specification at the first paragraph on page 4 beginning at line 7 in "clean" format, as follows:

--The pad is connected to the buffer circuit 6. The buffer circuit 6 has its output terminal connected to the juncture between the parasitic capacitances 3 and 4. The parasitic capacitance 3, as shown in Fig. 1, corresponds to a MOS capacitance created between the pad 1 and the island region 102. The parasitic capacitance 4 corresponds to a junction capacitance created between the island region 102 and the substrate. Thus, the output terminal of the buffer circuit 6 is connected to the island region 102.--

B1

Please amend the specification at the first paragraph on page 6 beginning at line 7 in "clean" format, as follows:

--Moreover, since it is not required to boost the drive capability of the buffer circuit 6, the parasitic capacitance 4 can be charged and discharged by the source current of the J-FET. The so-called J-FET source follower circuit can charge and discharge the parasitic capacitance 4. This makes it possible to use a combination of the J-FET 2 and the buffer circuit shown in Fig. 1. Fig. 2 shows an embodiment where the J-FET 2 and the buffer circuit 6 are used as one unit. Referring to Fig. 2, the source of the J-FET 2 produces and output signal and the source follower circuit of the J-FET 2 charges and discharges the parasitic capacitance 4. That is, the source of the J-FET 2 is connected to the island region 102 and the parasitic capacitances 3 and 4 are charged and discharged by the output of the J-FET 2. Referring to Figs. 1 and 2, the J-FET 2 is used as the input stage circuit of the integrated circuit. In addition, the circuit shown in Figs. 1 and 2 is applicable to an input stage circuit with a high input impedance, for example, an amplifier with a high input impedance including a buffer circuit.--

B2